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OPTIMIZATION OF TRANSISTOR DESIGN INCLUDING LARGE SIGNAL DEVICE/CIRCUIT INTERACTIONS AT EXTREMELY HIGH FREQUENCIES (20-100 + GHz)

Ralph Levy and H. L. Grubin
Scientific Research Associates, Inc.
50 Nye Road, P. O. Box 1058
Glastonbury, CT 06033

ABSTRACT

Transistor design for extremely high frequency applications requires consideration of the interaction between the device and the circuit to which it is connected. Traditional analytical transistor models are too approximate at some of these frequencies and may not account for variations of dopants and semiconductor materials (especially some of the newer materials) within the device. Physically based models of device performance are required. These are based on coupled systems of partial differential equations and typically require 20 minutes of Cray computer time for a single AC operating point. A technique is presented to extract parameters from a few partial differential equation solutions for the device to create a nonlinear equivalent circuit model which runs in approximately 1 second of personal computer time. This nonlinear equivalent circuit model accurately replicates the contact current properties of the device as computed by the partial differential solver on which it is based. Using the nonlinear equivalent circuit model of the device, optimization of system design can be performed based on device/circuit interactions.

INTRODUCTION

The evaluation of the potential performance of semiconductor devices for analog applications is usually performed in two ways. First, the device may be characterized through small signal admittance or scattering parameters which may be obtained by experiment for existing devices or by numerical simulation for a new device structure prior to fabrication. From these results, the devices can be characterized in terms of small signal parameters such as the unity gain cutoff frequency, f_t, and f_{max}. While these parameters provide a valid estimation of the limits of the device operation under linear, small signal conditions, such estimate will typically be in error under large signal conditions. Under large signal, high power conditions, nonlinear effects within the device become important. At low frequency, the nonlinear effects manifest themselves primarily as bias dependent parameters such as bias dependent transconductance and capacitance. At high frequency these parameters will also exhibit hysteresis effects due to the nonequilibrium nature of transport within the device.

As a result of these nonlinearities it is imperative that the performance of the device be evaluated while embedded in its operational circuit. It is the device-circuit interaction and resulting performance that is of interest and not simply the device characterization. Since it is obviously too costly and time consuming to design, fabricate and test a new device and then design, test, and redesign a circuit around the device in hope of achieving the desired performance, an alternative must be found. This alternative is numerical modeling. Funda-

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mentally, device-circuit interaction can be modeled using, equations to represent the device and coupling the external circuit to it through boundary conditions. While this has been and will continue to be done, it is presently too costly, even on the supercomputers available today, for all but the simplest of circuits. As a result, devices are approximated by nonlinear equivalent circuit elements in the large circuit simulation procedures. The adequacy of these equivalent circuit models has a direct impact on the predicted results.

In an effort to improve these device models Madjar and Rosenbaum [1] and Khatibzadeh and Trew [2] have developed procedures in which the FET is modeled by a system of nonlinear ordinary differential equations relating the gate and drain currents to the time dependent gate and drain voltages. The coefficients of these ODE's are determined **analytically**, using highly approximate models of the device. The present work is a significant generalization of the approach of [1] and [2]. Here the coefficients of the ODE's representing the device are determined **numerically**, through a physically based model; in this case the drift and diffusion equations and the moments of the Boltzmann transport equation. The resulting ODE representation is then executed, and the validity of the results are verified at select operating points. With such an agreement established, the equivalent circuit model can then be used with a higher degree of confidence in a complex circuit simulation and device/circuit optimization.

This study is based on three concepts. First the entire program is based on large signal concepts. Most large signal predictions of device performance are based upon small signal concepts; the assumption being that a 'good' small signal device is also a 'good' large signal device. Thus quantities such as the cutoff frequency, f_{max}, etc., have been used to assess device performance. However, this is not appropriate since the power requirements for MIMIC applications preclude small signal operation. MIMIC devices will be operated under large signal conditions, and large signal assessment of device performance is required.

Second, the computational device physics model is based on the drift and diffusion equations (DDE) for the 20-40 GHz range and on the nonequilibrium balance equations obtained from the first three moments of the Boltzmann transport equations (MBTE) for the 40-100$^+$ GHz range. The MBTE equations include the effects of carrier acceleration and velocity overshoot that are increasingly important as the frequency of interest increases and feature size decreases. Both analyses include the effects of processing parameters on device performance.

Third CAD compatibility was achieved by linking the DDE and MBTE analyses to nonlinear equivalent circuit analysis developed under a study sponsored by the National Science Foundation [3]. The nonlinear equivalent circuit model based on DDE or MBTE computed characteristics permitted very rapid (less than 1 second of Cray computer time) calculations of large signal AC performance of a device that accurately reproduced the more costly full calculations.

Coupling the nonlinear equivalent circuit model with the DDE and MBTE permits, for the first time a capability of performing fast and accurate calculations that describe device/circuit interactions. The nonlinear equivalent circuit model is compatible with commercially available CAD software and would run on a workstation. The nonlinear

equivalent circuit model has been coupled to a numerical optimization program and used to determine realistic goals for device/circuit performance.

Physical Modeling

The key element of the simulation is the system of partial differential equations used to describe the transient transport of electrons and holes in the devices. Drift and diffusion equations (DDE) are commonly used to describe transport in unipolar and bipolar devices. While these equations are valid at the low end of the frequency scale, they are incorrectly applied at higher frequency scales, typically those in the range of 40^+ GHz or when structural feature sizes are reduced. For GaAs based devices this is in the sub-2500 Å region. When DDE procedures are inadequate the procedures of choice involve either the moments of the Boltzmann transport equation (MBTE), or Monte Carlo (MC) methods. Both MBTE and MC procedures are computationally more intensive that DDE simulations. Unfortunately, Monte Carlo algorithms require the most intensive computational resources, and are not presently practical for a CAD environment.

A brief description is now presented of the DDE and MBTE analyses and how SRA's nonlinear equivalent circuit analysis is based on the results of the MBTE calculations.

Semiconductor Drift and Diffusion Equations

The governing drift and diffusion equations are the continuity equations for electrons and holes and Poisson's equation:

$$\frac{\partial N}{\partial t} = \nabla \cdot \left[-N\mu_n \nabla(\psi+\psi_n) + D_n \nabla N \right] + G - R \qquad (1)$$

$$\frac{\partial P}{\partial t} = \nabla \cdot \left[P\mu_p \nabla(\psi+\psi_p) + D_p \nabla P \right] + G - R \qquad (2)$$

$$\nabla \cdot \epsilon \nabla \psi = e(N - N_D - P + N_A) \qquad (3)$$

where N and P are the electron and hole concentrations, respectively, and e is the electron charge. The quantity within the square brackets represents the electron and hole currents densities, $-J_n/e$ and J_p/e, respectively, G represents generation, R recombination, ψ is the potential, ϵ the permittivity, and N_D and N_A are the concentrations of donors and acceptor ions, respectively. The terms ψ_n and ψ_p are introduced to account for variations in the conduction and valence band energy levels. Through ψ_n and ψ_p such effects as band gap narrowing and heterojunctions may be accounted for.

Within the context of equations (1) through (3) materials such as gallium arsenide are represented by field dependent mobilities with a region of negative differential conductivity (NDC). While NDC is included in the subject analysis we point out that it is a feature never included in the analytical representations of nonlinear devices.

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Moments of the Boltzmann Transport Equations

It is now commonly accepted that the major inadequacy of the drift and diffusion equations is the use of equilibrium field dependent velocity relationships. Its usage is a statement that acceleration is to be ignored. The MBTE overcomes this inadequacy.

The nonequilibrium MBTE are obtained by taking the moments of the Boltzmann transport equation with respect to carrier density, momentum and energy. This yields a set of governing equations which are similar in form to the equations utilized for multi-phase flow in fluid dynamics. The governing equations reflect the conservation, or balance laws of carrier density, carrier momentum and carrier energy and are written down for two species of electrons namely, the central (small effective mass) and satellite (large effective mass) valley carriers and one type of hole. Incorporation of holes is both for breakdown consideration as well as for the possibility of buried 'p' layers in the design of FETS. The balance equations follow.

Carrier Balance (or equations of continuity):

$$\partial n_1/\partial t = -\nabla\cdot(n_1\mathbf{V}_1) - n_1\Gamma_1 + n_2\Gamma_2 - R \tag{4}$$

$$\partial n_2/\partial t = -\nabla\cdot(n_2\mathbf{V}_2) + n_1\Gamma_1 - n_2\Gamma_2 \tag{5}$$

$$\partial n_3/\partial t = -\nabla\cdot(n_3\mathbf{V}_3) - R \tag{6}$$

where n_1 and n_2 are the central valley and satellite valley carrier number densities respectively while $\mathbf{V}_1$ and $\mathbf{V}_2$ are the corresponding velocities. Γ_1 and Γ_2 are the corresponding scattering rates for particle conservation. Γ_1 represents scattering of carriers from the Γ valley to the L valley in GaAs. Γ_2 is the return rate. R represents the net recombination of electrons and holes, assumed to occur only through the Γ valley electrons. n_3 and $\mathbf{V}_3$ are the number density and velocity of holes.

Momentum Balance (Newton's Law) for the Central Valley:

$$\partial(n_1\mathbf{P}_1)/\partial t + \nabla\cdot(n_1\mathbf{V}_1\mathbf{P}_1) + n_1\mathbf{P}_1\Gamma_3 = -n_1e\mathbf{F}_n - \nabla\wp_1 - \nabla\cdot\sigma_1 + n_1[\mathbf{V}_1.\mathbf{V}_1/2 + T_1/m_1]\nabla m_1 \tag{7}$$

where there is a force contribution due to spatial variations in the effective mass. In the above the momentum, $\mathbf{P}_1$, and the field, $\mathbf{F}_n$, are defined by

$$\mathbf{P}_1 \equiv m_1\mathbf{V}_1 \tag{8}$$

$$\mathbf{F}_n = -(\nabla\psi + \nabla\chi/e) \tag{9}$$

m_1 is the mass of the central valley carrier, e is the electronic charge, ψ is the electric potential and χ is the electron affinity. $\mathbf{F}$ is the field due to potential differences and conduction band discontinuity arising from material variations. The partial pressure, $\wp_1$, is

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related to the central valley carrier temperature, T_1, and number density by the perfect gas relationship, which results from the assumption of Boltzmann statistics,

$$p = n_1 k T_1 \tag{10}$$

where k is Boltzmann's constant. Γ_3 is the scattering rate for the central valley carrier momentum. Contributions to Γ_3 include impurity, acoustic phonon, polar phonon, nonpolar intervalley scattering. The effects of electron-hole scattering is accounted for through an enhancement of the impurity scattering. The term $\nabla:\sigma_1$ represents the stress forces. In this study, the stress tensor, σ_1, is approximated by the relationship

$$\sigma_1 = \eta_1 \nabla V_1 \tag{11}$$

where η_1 is the viscosity associated with the central valley carriers. Similar momentum conservation equations can be written for the satellite valley and for holes.

Energy Balance for the Central Valley Carriers:

There are various forms in which the central and satellite valley carrier energy equations can be described. We choose to cast the energy equations in terms of the central and satellite valley temperatures, T_1 and T_2.

$$\begin{aligned} &\partial(n_1 T_1)/\partial t + \nabla\cdot(n_1 V_1 T_1) + (n_1 T_1 \Gamma_5 - n_2 T_2 \Gamma_6) = \\ &\quad -2/3[n_1 T_1 \nabla\cdot V_1 + \sigma_1:\nabla V_1/k - \nabla\cdot(\kappa \nabla T_1)/k] \\ &+ 3V_1\cdot V_1 m_1[n_1(2\Gamma_3 - \Gamma_1) + n_2\Gamma_2] - n_1 V_1 T_1/m_1\cdot\nabla m1 \end{aligned} \tag{12}$$

In equation (12) Γ_5 denotes energy relaxation within the central valley **plus** energy exchange with the satellite valley; Γ_6 denotes energy exchange between the satellite and central valley. All energy exchange between electrons and holes is ignored. A similar energy conservation equations can be written for the satellite valley electrons and for holes. In the energy balance equation for electrons and holes equations the contribution of the recombination have not been included.

The potential is related to the total number density through Poisson's equation

$$\nabla\cdot\epsilon\nabla\psi = e[(n_1 + n_2 - n_0) - (n_3 - p_0)] \tag{13}$$

where n_0 is the donor density, p_0 is the acceptor density and ϵ is the permitivity.

In two dimensions, the complete problem description requires 13 equations consisting of 3 continuity equations, 6 momentum equations, 3 energy equations and a Poisson's equation. The boundary conditions for potential are the same as used for the drift and diffusion equations. At ohmic contacts, the boundary condition is given by the sum of the applied bias and an appropriate built-in potential. The temperature of all carriers are assumed to be at 300K at the ohmic contacts. The carrier densities at the contacts are fixed at the value of local doping. For velocities, the normal gradient is taken to be zero.

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Consideration of the External Circuit

Typically, in device simulations the voltage at the contacts are either fixed at a constant value or a time dependence is specified. When an external circuit is introduced, the voltage on the contact is determined by solving the device equations along with the circuit equation. The external circuit thus represents a boundary condition as far as the device simulation is concerned.

Transition of the Device/Circuit Results to Systems and Circuit Engineers.

The present study was predicated in two facts: (1) While the ideal way to transition the technology of device physics and device-circuit interactions is to deliver to the systems engineer a time dependent code that incorporates all of the partial differential equations describing the device, and the ordinary differential equations describing the circuit, the long run times generally associated with solving both the DDE and MBTE algorithms, rendered this approach impractical for engineers. (2) The approach favored by engineers to allow practical device-circuit interfacing is to obtain analytical representations of the dc current voltage characteristics of a given three terminal device, as well as analytical approximations for the relevant capacitances of the device, and then lump these parameters into a large signal simulator that solves the following set of coupled ordinary differential equations [3]:

$$I_g(t) = I_{g_o}[V_g(t),V_d(t-t_1)] + C_{gg}\, dV_g(t-t_2)/dt + C_{dg}\, dV_d(t)/dt \qquad (14)$$

$$I_d(t) = I_{do}[V_g(t-t_0),V_d(t)] + C_{gd}\, dV_g(t)/dt + C_{dd}\, dV_d(t-t_2)/dt \qquad (15)$$

In the above the terms t_0, t_1, t_2, represent time delays associate with transit of carriers between the gate and drain, drain and gate, and source and gate, respectively. The capacitive contributions are functions of the gate and drain voltage, with the time delays appropriate to the equation in which they appear. Equations of the type represented by equations (14) and (15), which are "SPICE"-like equations, are then typically coupled to harmonic balance programs.

Application of standard numerical optimization techniques with two-dimensional systems of partial differential equations (DDE or MBTE) is conceptually straightforward. However, implementation requires large computer resources, making it of limited interest to device designers at this time. Use of the equivalent circuit analysis, equations (14) and (15), results in very fast calculations that could be performed rapidly on a personal computer. The issue then becomes the accuracy of the equivalent circuit model. Other researchers [1] and [2] determine the coefficients and time delays from analytical considerations. This is a useful approach for device designs and materials in operating regimes that are well understood. The intent of the present work is to extend the utility of the equivalent circuit model to materials, designs and operating conditions that are not well understood. To achieve this goal the coefficients and time delays for equations (14) and (15) are derived from solution of two-dimensional systems of partial differential equations. This procedure obviates the need to make approximations that permit analytical expressions to be written for the coefficients and time delays in (14) and (15). It also permits extension of the analysis to other device designs and complex doping distributions.

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The procedures for obtaining the terms relevant to equations (14) and (15);

$$C_{gg}, C_{dg}, C_{gd}, C_{dd}, t_0, t_1, t_2$$

involves five broad steps. These are identified below.

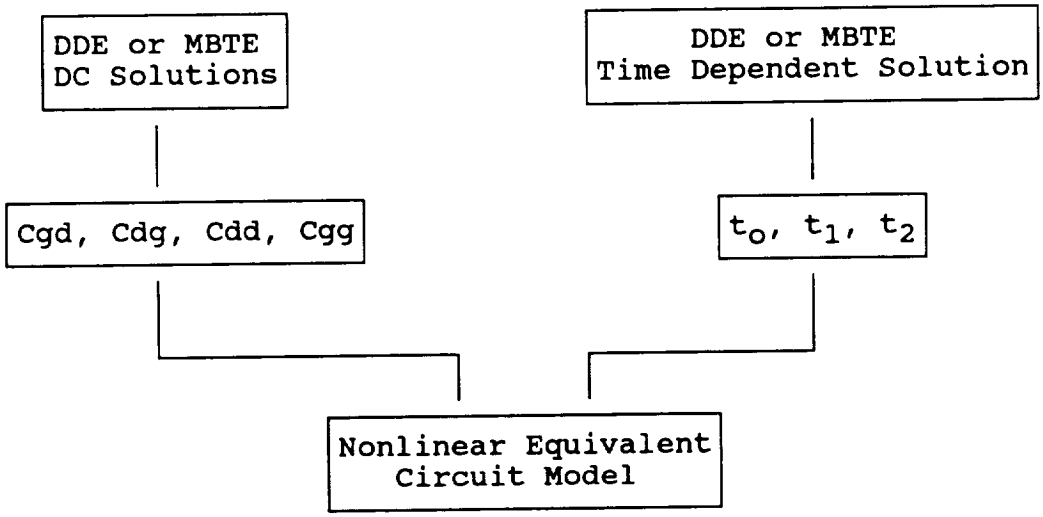
(1) From the DDE or MBTE algorithm the dc characteristics of the device are obtained.

(2) Perturbations of the dc characteristics are obtained as a function of gate and drain voltage. Small changes in the net charge on the drain and gate contacts are computed as a function of changes in gate voltage on the gate contact; leading to values for C_{gg} and C_{gd}. A similar procedure yields involving changes in drain voltage lead to values of C_{gd} and C_{dd}.

(3) Time dependent calculations demonstrate that there are transit time delays associated with the imposition of a signal on the gate contact and its observation on the drain contact. Similarly a change in voltage on the drain contact will have its effect on the gate contact delayed. Time dependent DDE or MBTE calculations are performed and the time delays associated with this are represented by the terms t_0 and t_1. Time delay associated with the source-gate loop is represented by t_2.

(4) The above parameters are incorporated onto the ODE solvers of equations (14) and (15).

A flow chart describing the above is shown below.



The advantage of the ODE solver over that which incorporates solutions to the partial differential equations is **engineering time**. A system of ODE solvers that can be used to replicate the output of the two-dimensional physically based models could be effectively used by circuit engineers to represent the device in circuit codes. It is worthwhile noting

that alternative formulations for fast calculations can be considered; e.g., quasi two-dimensional analysis of Snowden and Pantoja [4]. To use such an analysis, the predictions would be calibrated against an MBTE solution for the operating conditions of interest.

RESULTS

The above equivalent circuit model was compared to the drift and diffusion calculation of the FET of figure 1 in AC operation at 20, 40 and 60 GHz with a resistive load on the drain. Lissajous of these calculations are presented in figures 2 and 3. Comparisons of three power gain calculations at the same frequencies are shown in table 1. The lissajous, after the initial transient, and the AC power calculations are well represented by the equivalent circuit analysis.

Large Signal Circuit Dependent Results at 94 GHz

Large signal circuit dependent operation at 94 GHz was studied by connecting a 0.25 micron gate FET to a resistive load as shown in Figure 4. The drain battery voltage was set at 3 volts. Since the computed current levels in the device were dependent on the analysis used, the resistor was sized to have a one volt drop under DC conditions for a gate width of 300 microns. A sinusoidal voltage was applied to the gate at an amplitude of 0.5 volts and a frequency of 94 GHz. The gate and drain voltages and currents are presented in figure 8 as a function of time. The computed contact currents become periodic in time (steady AC) in less than one cycle and show sinusoidal periodic behavior at all contacts. Nonlinear effects which manifest themselves in gain compression, were not apparent at this gate bias level.

Nonlinear Equivalent Circuit Analysis at 94 GHz

The nonlinear equivalent circuit analysis of the recessed gate FET was implemented based on the MBTE calculations. Curve fits were obtained for I_d (Vg, Vd) and for the capacitive coefficients in equations 14 and 15. Figure 5 and 6 show the equivalent circuit results in the same form as the MBTE calculations. The lissajous are seen to have the same shape and similar harmonic content. It should be noted that while the MBTE calculation required twenty-five minutes of Cray Supercomputer time the Nonlinear Equivalent Circuit Analysis required less than one second of time on a personal computer.

Load Pull Calculations at 94 GHz

To demonstrate the ability to perform load pull simulations, such a calculation was performed by applying a sinusoidal signal at the gate with a magnitude of 0.5 volts. A sinusoidal voltage was applied to the drain with a magnitude of 0.6 volts and a phase lag of 200° behind the gate signal. This calculation was performed using the DDE, MBTE and the SRANEC analysis based upon the MBTE parameters. Figure 7 shows the Vg-Vd lissajous figure for these three calculations. Figure 8 compares the computed output for the load pull for each analysis. Note again the significant differences between the DDE and the MBTE calculations.

To demonstrate the utility of the equivalent circuit model an optimization program was mated to the **equivalent** circuit model. The optimization program drove the gate and drain voltages sinusoidally with an imposed phase delay:

$$V_g = V_g^o + \Delta V_g \sin(\omega t) \qquad (16a)$$

$$V_d = V_d^o + \Delta V_d \sin(\omega t - \phi) \qquad (16b)$$

The following optimization problem was posed: For fixed $V_g{}^o = -2$ volts, $V_d{}^o = 4$ volts and $\Delta V_d = 1$ volt what values of ΔV_g and ϕ will provide a power gain of 8 db at an input power of 10^{-2} watts. ΔV_g was constrained to be in the range $0 \leq \Delta V_g \leq 1.5$ volts. This problem was solved at a series of frequencies from 10 GHz to 50 GHz using a Quasi-Newton optimization procedure with BFGS updating. For frequencies from 10 to 20 GHz the desired power gain of 8 db was achieved. Above 20 GHz the power gain decreased as a function of frequency as shown in figure 9. Solution of the above problem at each frequency required 30 to 90 AC device calculations. This would be unreasonably time consuming and expensive for a drift and diffusion analysis even on modern supercomputers. Using the equivalent circuit model each optimization requiring 30-90 AC steady state device calculations took approximately 1 minute of time on an IBM PC.

CONCLUSIONS

Using physically based research algorithms a nonlinear equivalent circuit analysis of a transistor operating at extremely high frequencies (20-100+ GHz) can be generated. The nonlinear equivalent circuit model reproduces transistor contact current in less than one second of computer time that required approximately 20 minutes of Cray supercomputer time suing the full physically based models. With this accuracy and concurrent run time advantage, tranditional optimizatiton techniques can be brought to bear on the device/circuit interaction problem.

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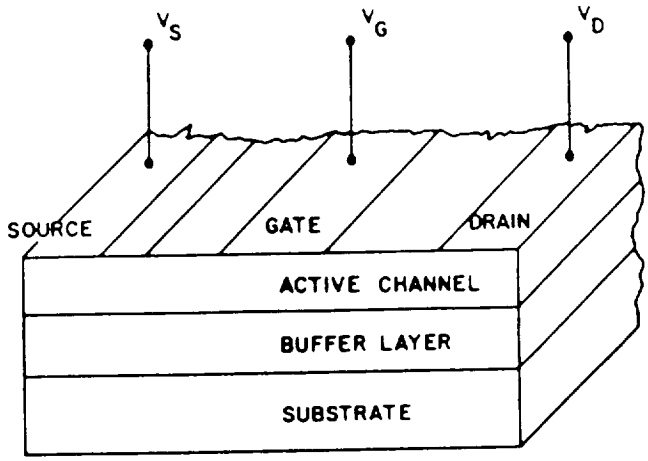

Figure 1. FET Schematic from Reference 5.

PHYSICAL PARAMETERS FOR THE 0.5 μm GATE LENGTH GaAs MESFET USED IN THE SIMULATION	
GATE LENGTH	0.55 μm
GATE WIDTH	300 μm
CHANNEL THICKNESS	0.15 μm
SOURCE TO GATE SPACING	0.5 μm
DRAIN TO GATE SPACING	0.6 μm
BUFFER LAYER THICKNESS	0.2 μm
GATE METALLIZATION	ALUMINUM
SCHOTTKY BARRIER HEIGHT	0.80 V
TEMPERATURE	350 K
DOPING OF ACTIVE LAYER	1.5×10^{23} m^{-3}
DOPING AT CONTACTS	3.7×10^{23} m^{-3}
SUBSTRATE IMPURITY LEVEL	1.0×10^{23} m^{-3}

Table 1.

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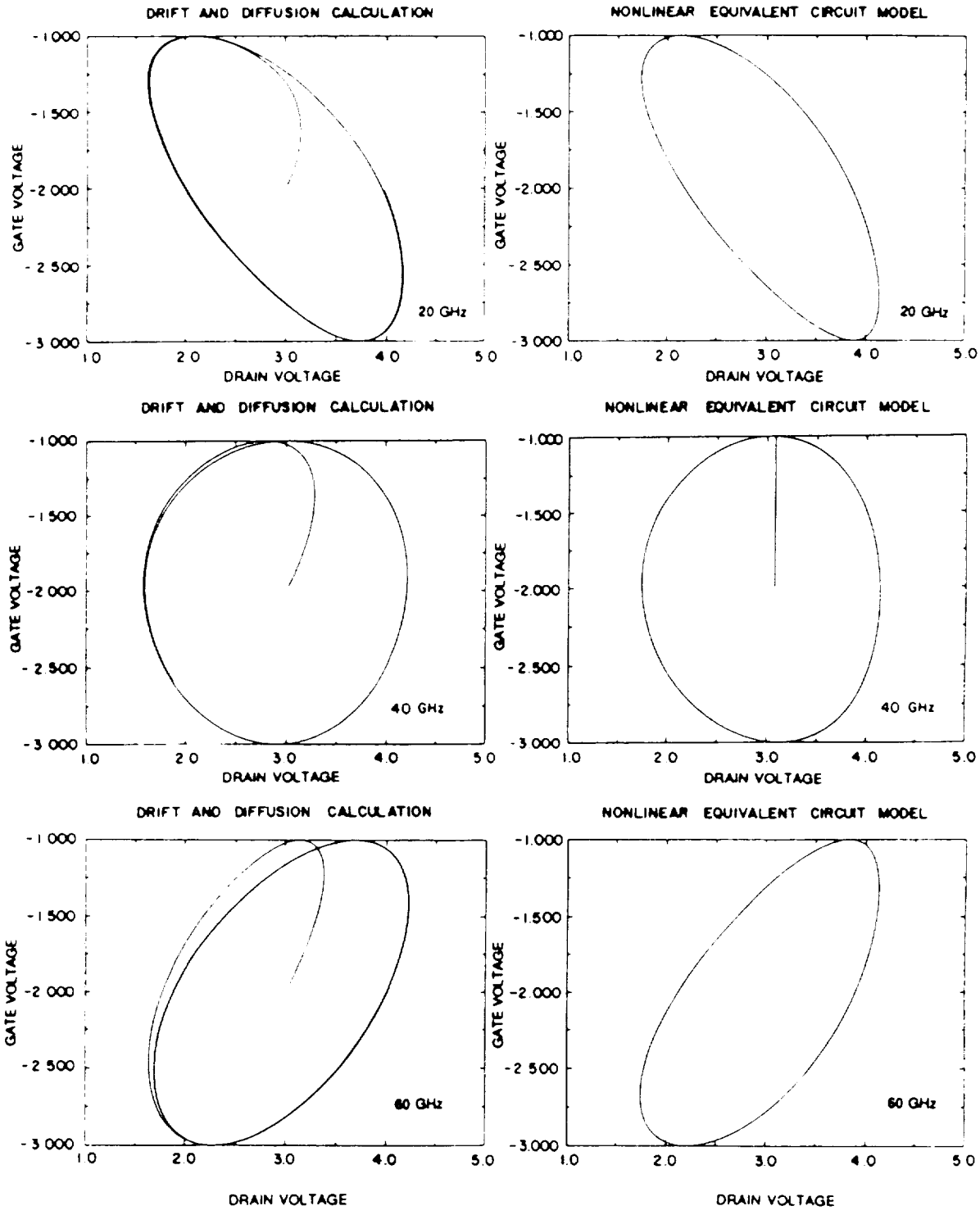

Figure 2. V_g - V_d Lissajous Comparison.

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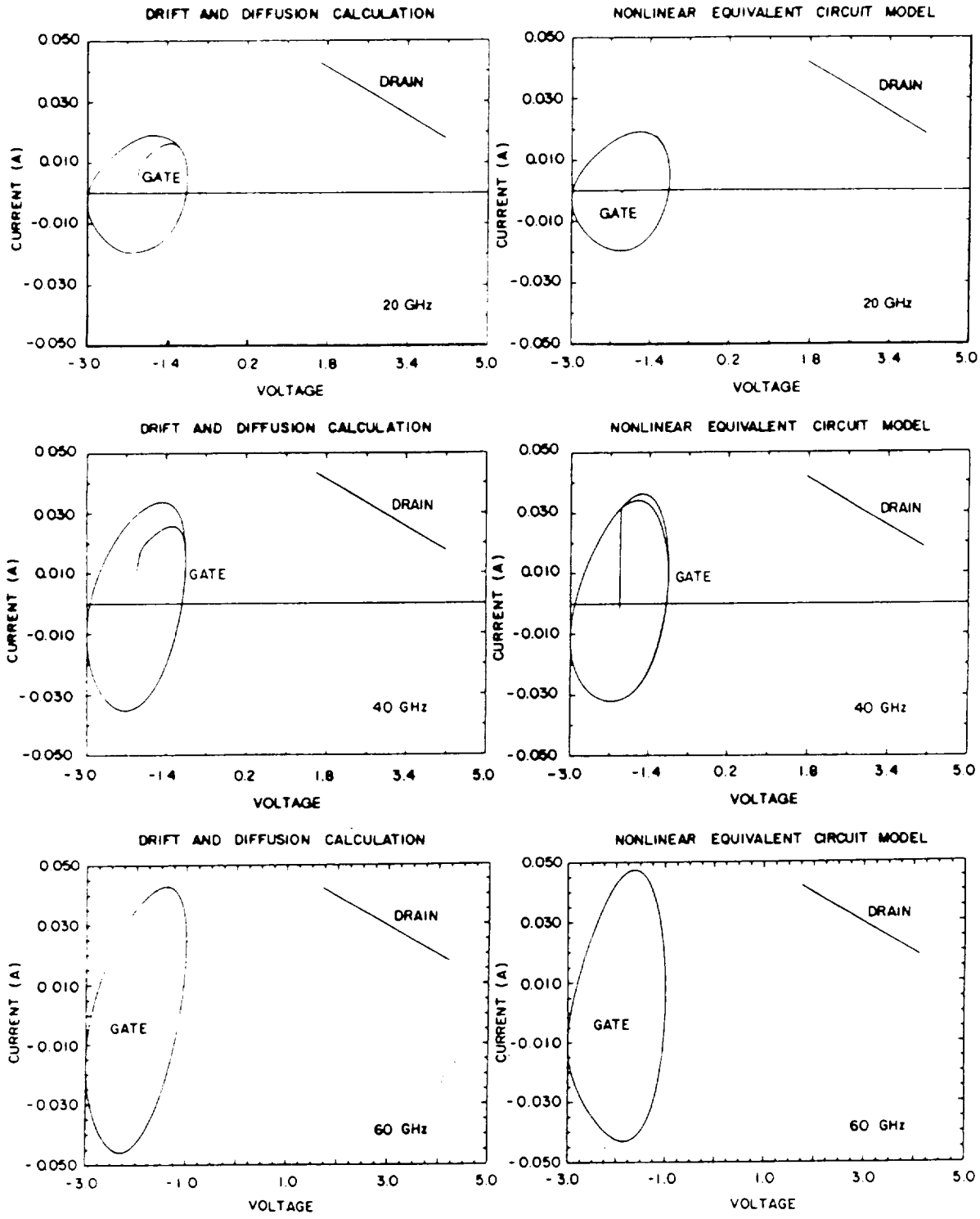

Figure 3. I-V Lissajous Comparison.

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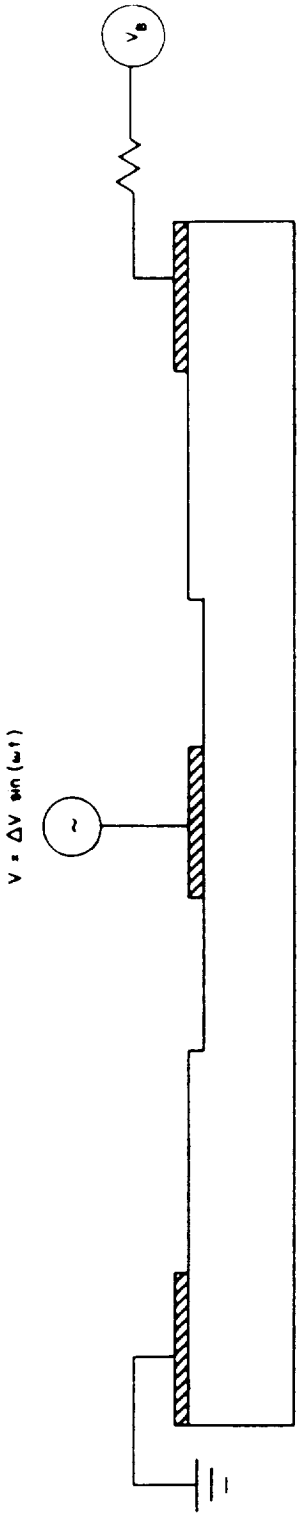

Figure 4. Schematic of FET with Resistive External Load.

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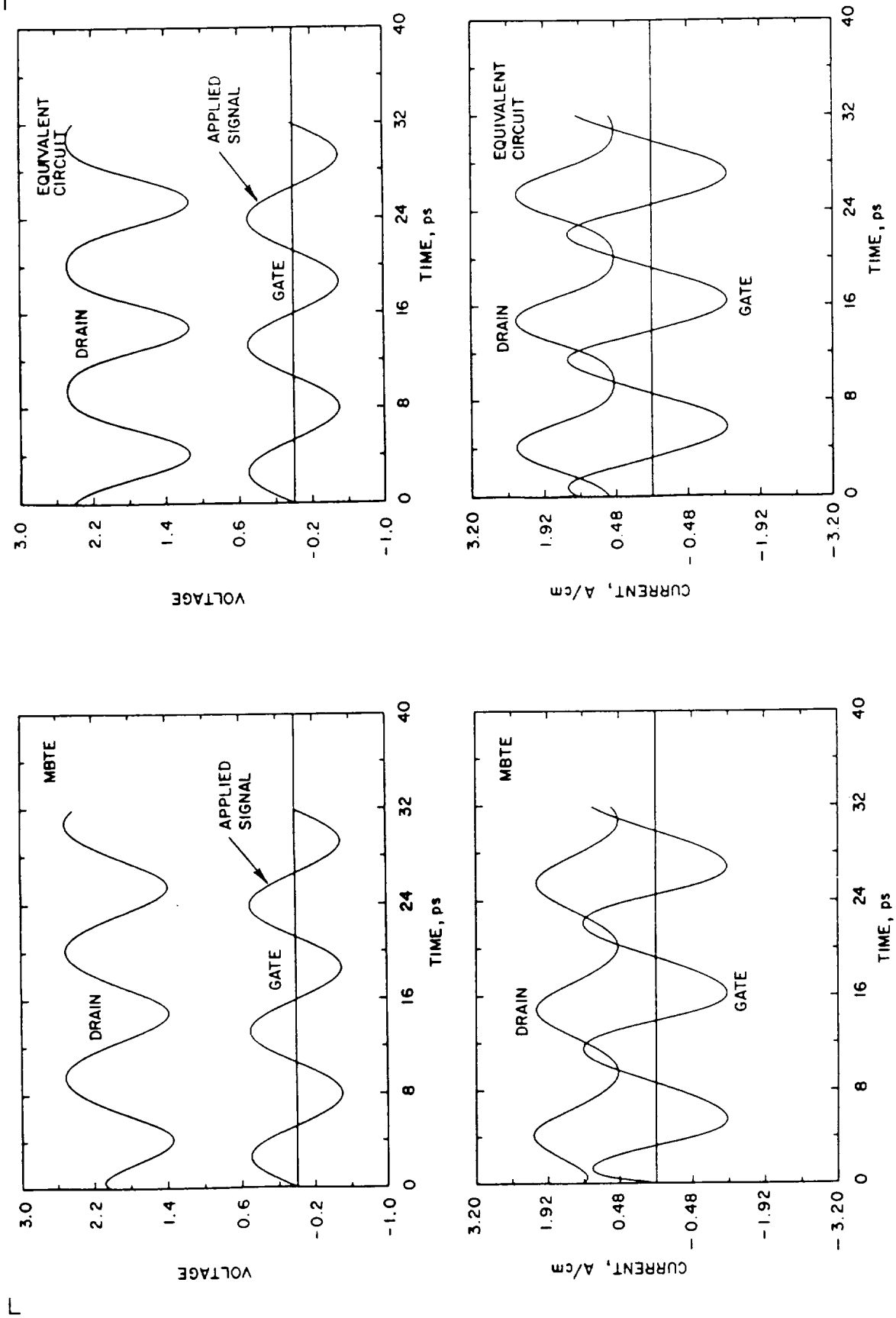

Figure 5. MBTE and Nonlinear Equivalent Circuit Gate and Drain Contact Large Signal Voltage and Current as a Function of Time at 94 GHz.

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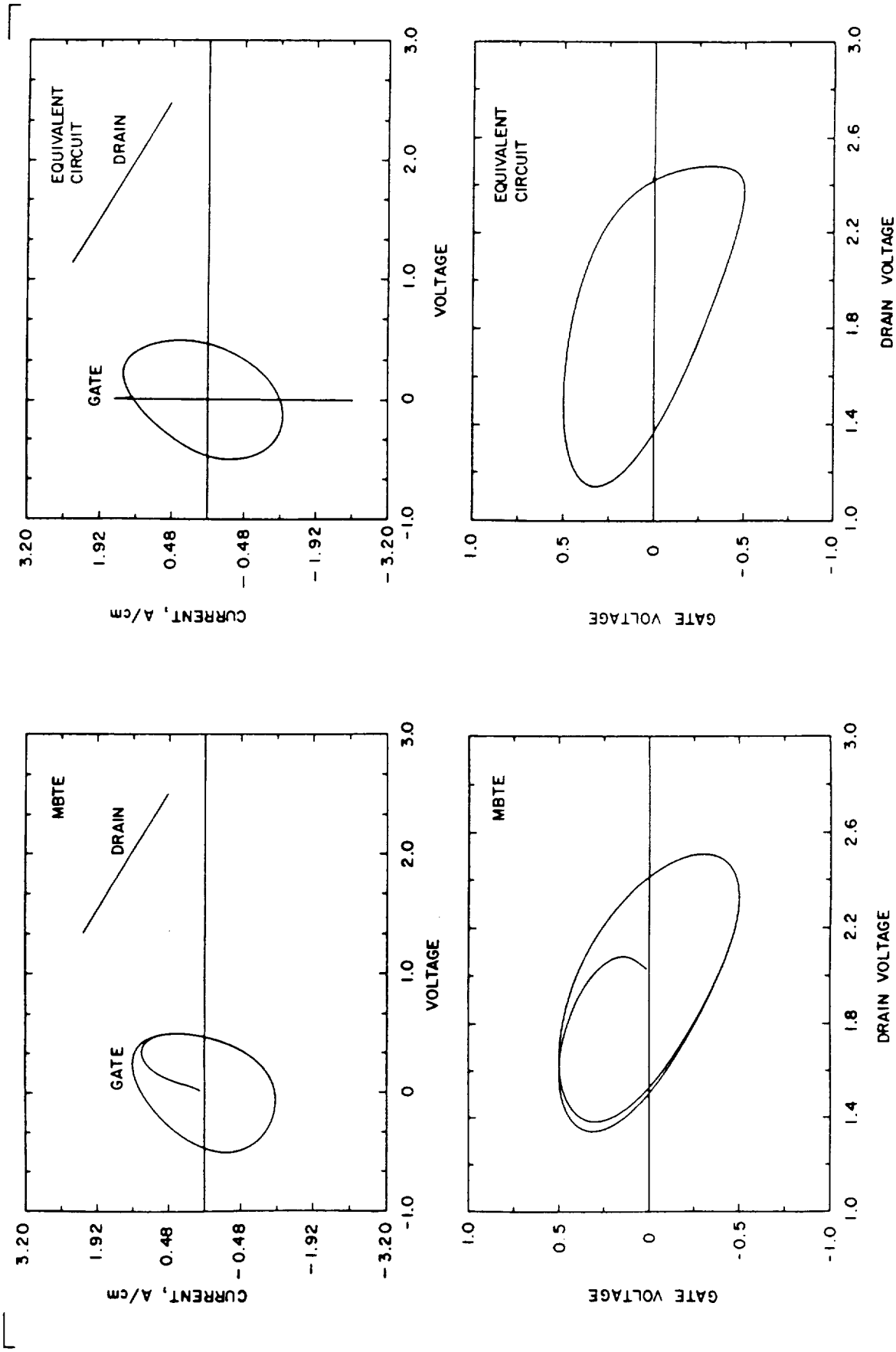

Figure 6. Large Signal Lissajous (MBTE and Nonlinear Equivalent Circuit) at 94 GHz.

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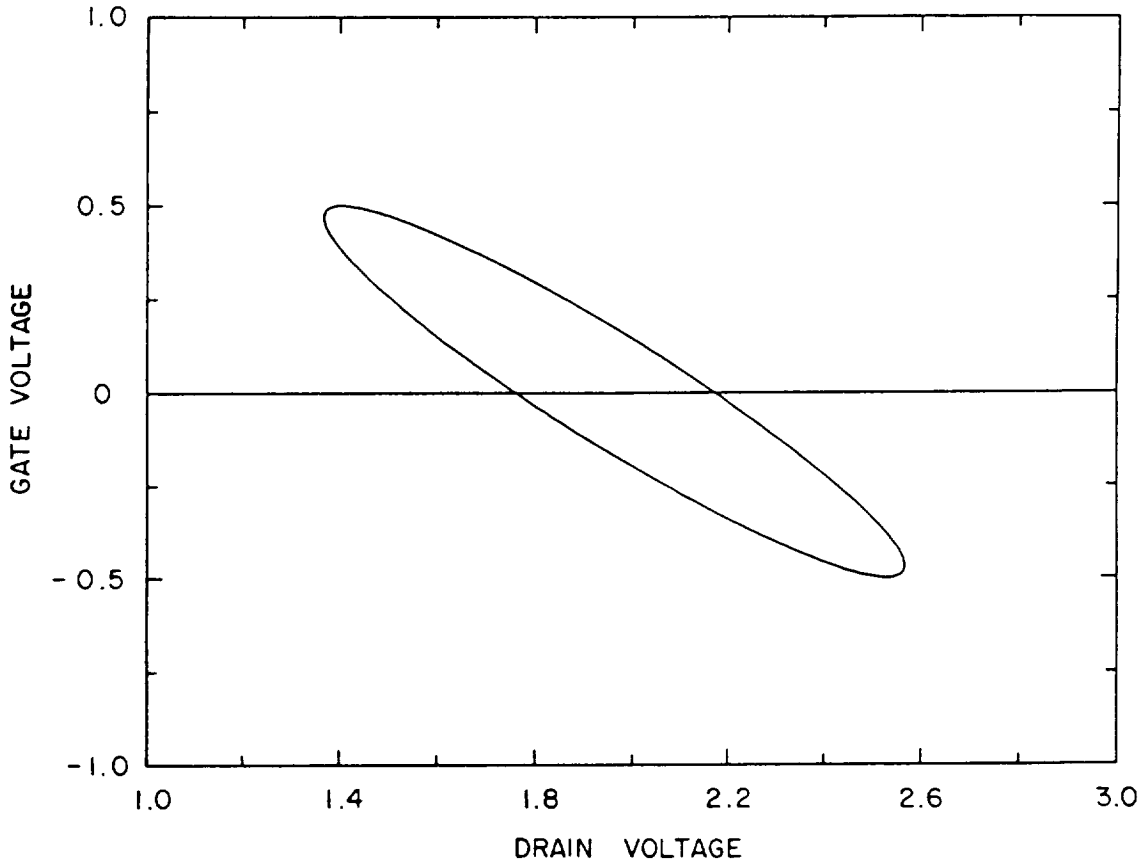

Figure 7. V_g - V_d Lissajous of Applied Signal in Load Pull Calculations at 94 GHz.

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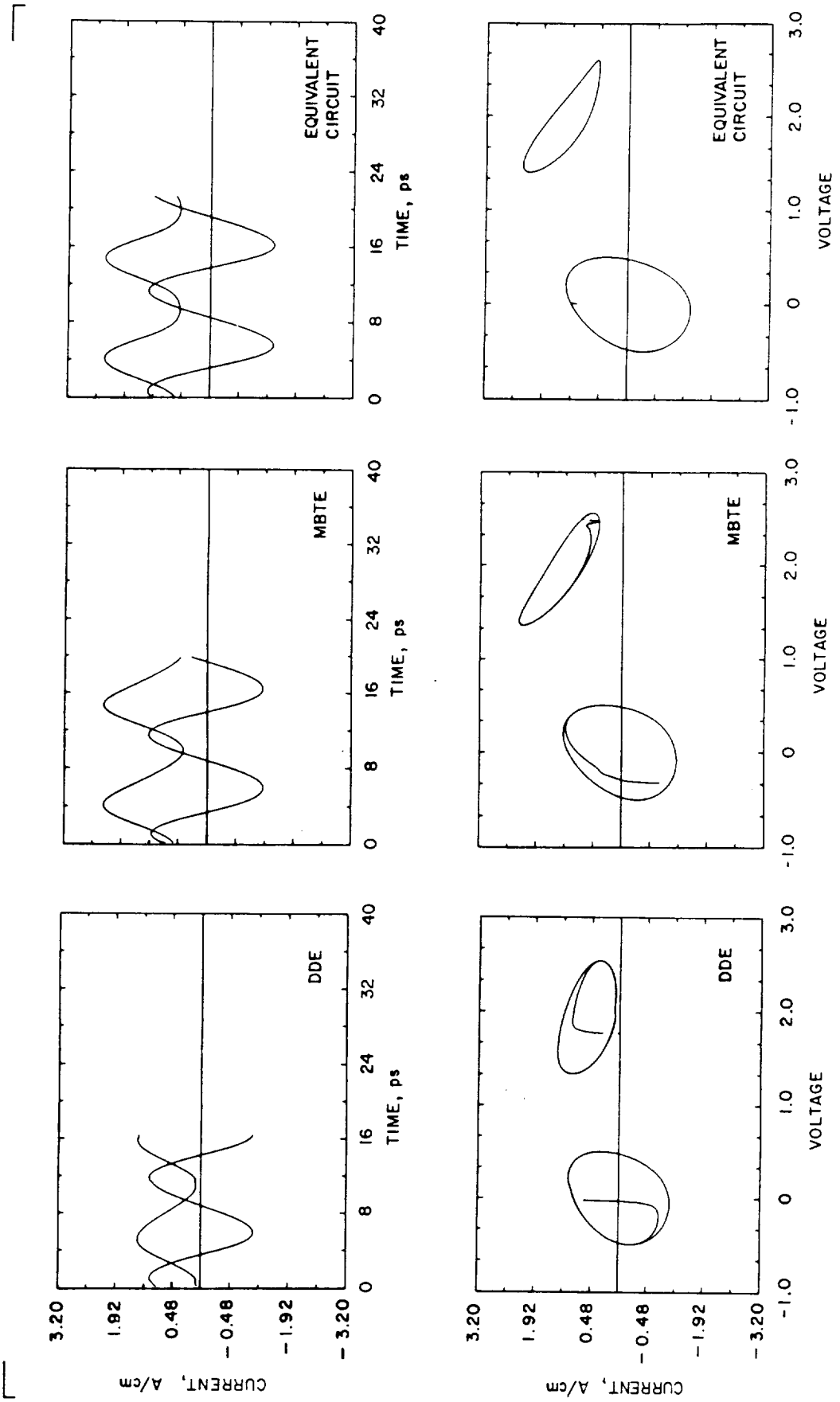

Figure 8. Load Pull Calculations Gate and Drain Contact Current versus Time and Gate and Drain I-V Lissajous at 94 GHz.

Third International Conference on Inverse Design Concepts and Optimization in Engineering Sciences (ICIDES-III), Editor: G.S. Dulikravich, Washington D.C., October 23-25, 1991.

	DRIFT AND DIFFUSION CALCULATION	NONLINEAR EQUIVALENT CIRCUIT MODEL
20 GHz	3.92	4.03
40 GHz	1.32	1.25
60 GHz	0.78	0.80

Table 2. Ratio of Output Power to Input Power - Comparison of Drift and Diffusion Calculation and Nonlinear Equivalent Circuit.

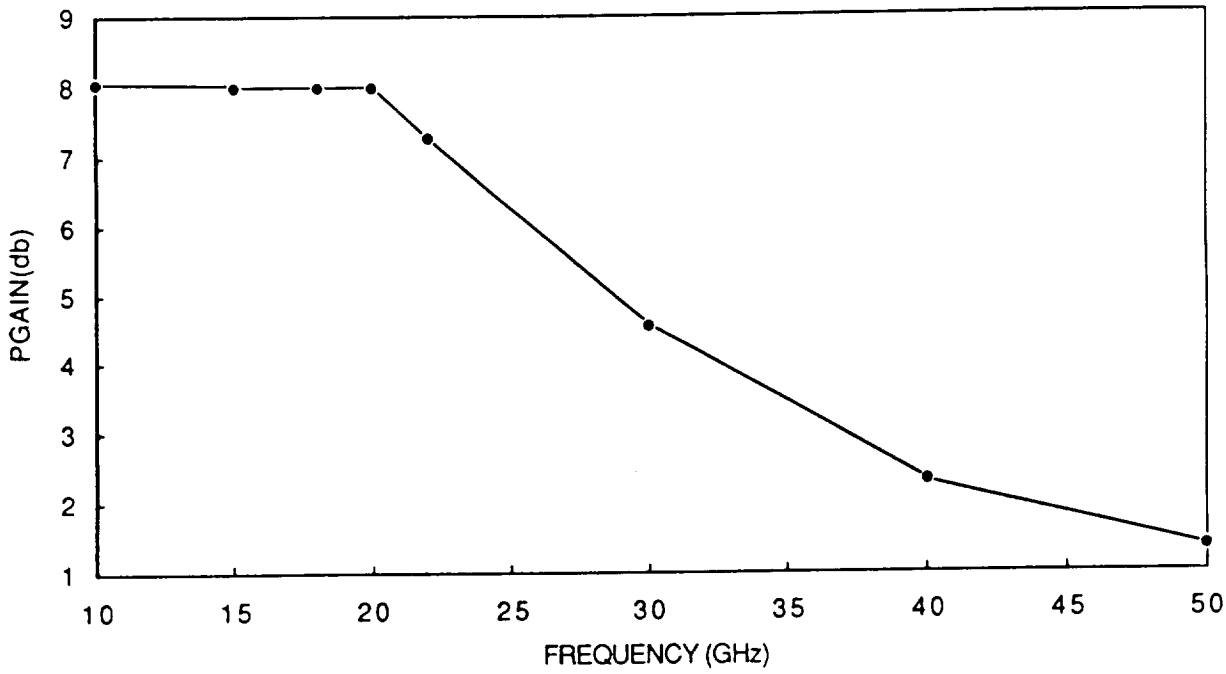

Figure 9. AC Power Gain versus Frequency at Fixed Input AC Power.